



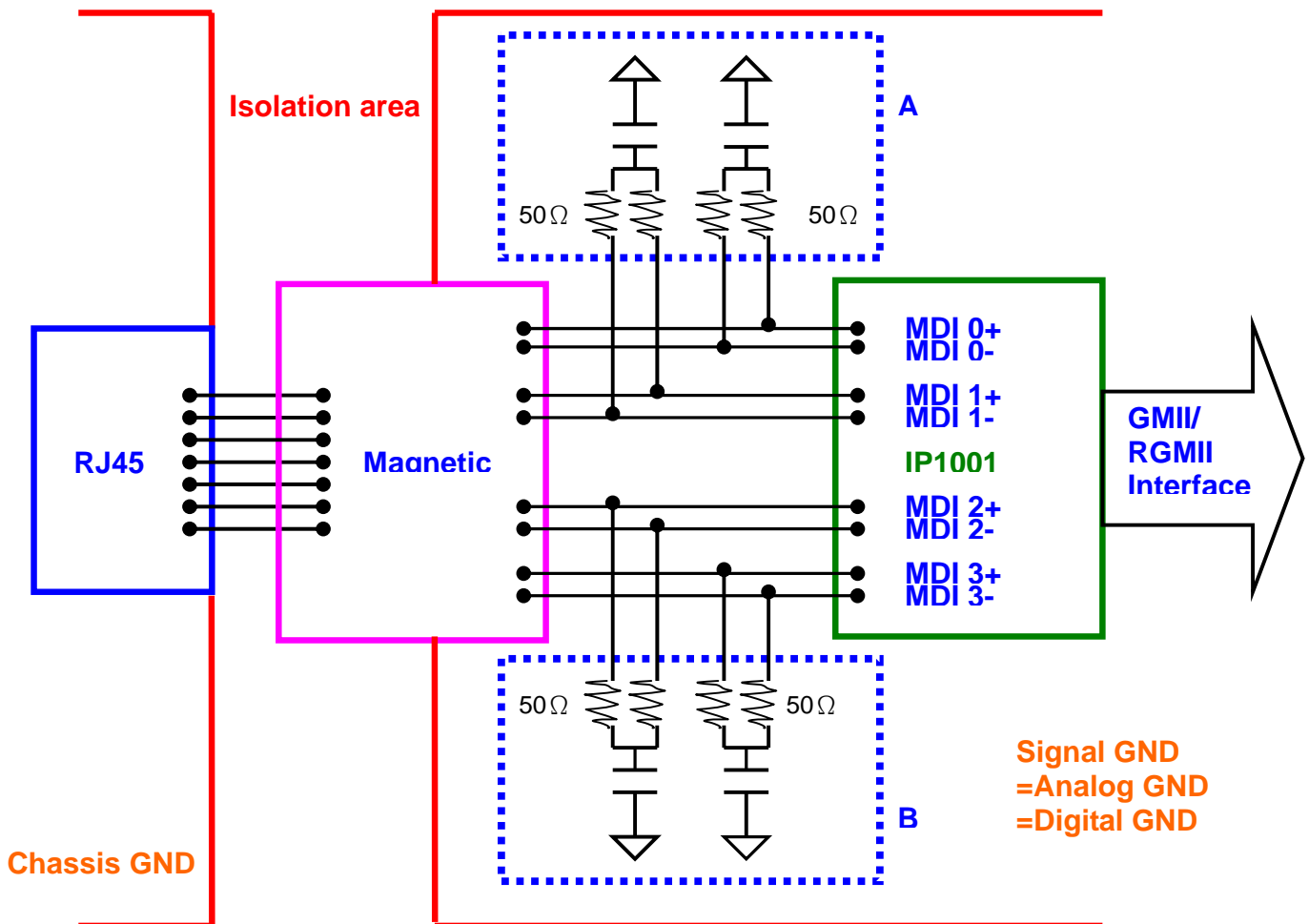
Index

1	Purpose	2
2	Magnetic trace routing.....	2
3	Power Supply Plane & GND Plane	3
4	PHY interface	3
5	Trace routing & Placement	3
6	ESD protection	3
7	EMI Supression.....	3

1 Purpose

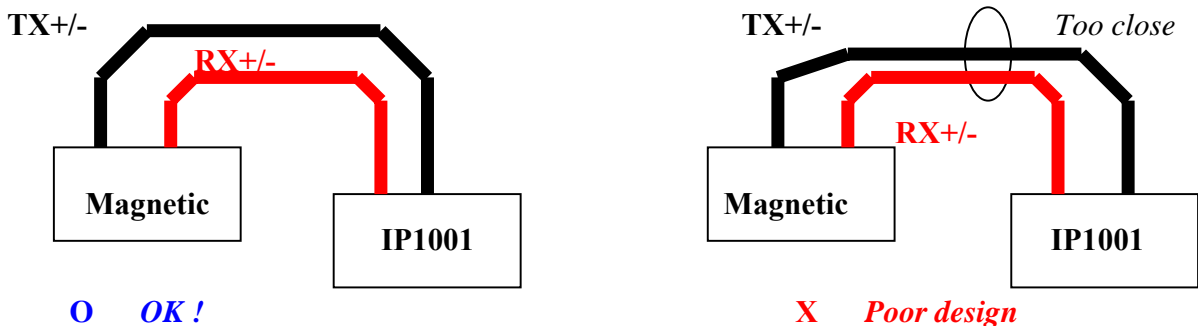
- (1) Make a stable environment for IP1001 LF working
- (2) Improve EMI & EMC performance
- (3) Make better ESD protection

2 Magnetic trace routing



- The termination resistors ($50\Omega \pm 1\%$ in block A & B) should be placed as close to magnetic as possible. For better impedance matching, please
 - (1) Pay attention to the termination resistors and caps layout.
 - (2) Avoid vias and layer changes.

- Try to keep the distance between TX+/- & RX+/- differential pairs far for good isolation. When these two pair of traces in parallel, don't place them too close to avoid unwanted interference. Shielding with GND planes can get a better isolation to these two differential pairs.



3 Power Supply Plane & GND Plane

- No power and GND planes can be underneath the isolation area between the RJ-45 connector and magnetic. Connect the isolation GND to the Chassis GND.
- Try to keep the GND plane as large as possible, and do not partition the GND plane to keep good GND return path.
- It will be better to place analog power to one block and digital power to the other block. Even though the supply voltage of analog power and the supply voltage of digital power is identical, it is recommended to separate both power supply with ferrite bead or 0Ω resistor.

4 PHY interface

- Try to use via as less as possible on GMII/RGMII interface traces to minimize the timing skew. Keep GMII/RGMII interface traces less than 6 inches long, minimizing the interface timing skew.
- For TX part of RGMII/GMII, it's advised to keep the difference of the trace length less than 400 mils among the TX part. This rule can be applied to Rx part of RGMII/GMII.

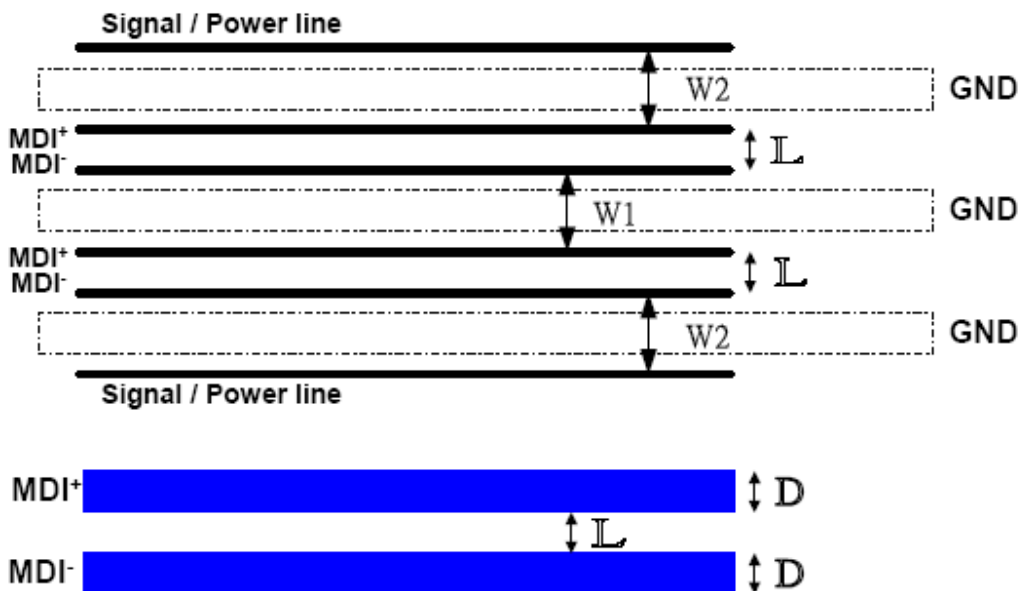
5 Trace routing & Placement

To reduce the propagation delay, frequency noise, crosstalk and improve the signal quality that IP1001 LF receives, and reduce the loss of the transmit signals. Please follow the following suggestions.

- Avoid right angle signal trace:



- The traces from the crystal to IP1001 should be short and should not be placed close to high-frequency devices, GMII/RGMII interface signals, Tx+/-, Rx+/- traces, edge of PCB board, power plane and magnetic devices.
- For T_x , R_x traces:
 - ➔ T_x+ & T_x- should be equal in length (If possible) to each other.
 - R_x+ & R_x- should be equal in length (If possible) to each other.
 - ➔ The line width and distance between T_x and R_x :





D: Line width is as wide as possible in the range of (6mils ~ 12 mils), ex: 8mils.

L: Width between MDI+ and MDI- should be small, ex: 4mils. **If possible,*

D=L=8mils(3-W rule) is good layout for MDI trace.

W1: Isolation width between each pair is as wide as possible, ex: 30mils.

Use GND plane to guard TX pair and RX pair to improve the EMI performance.

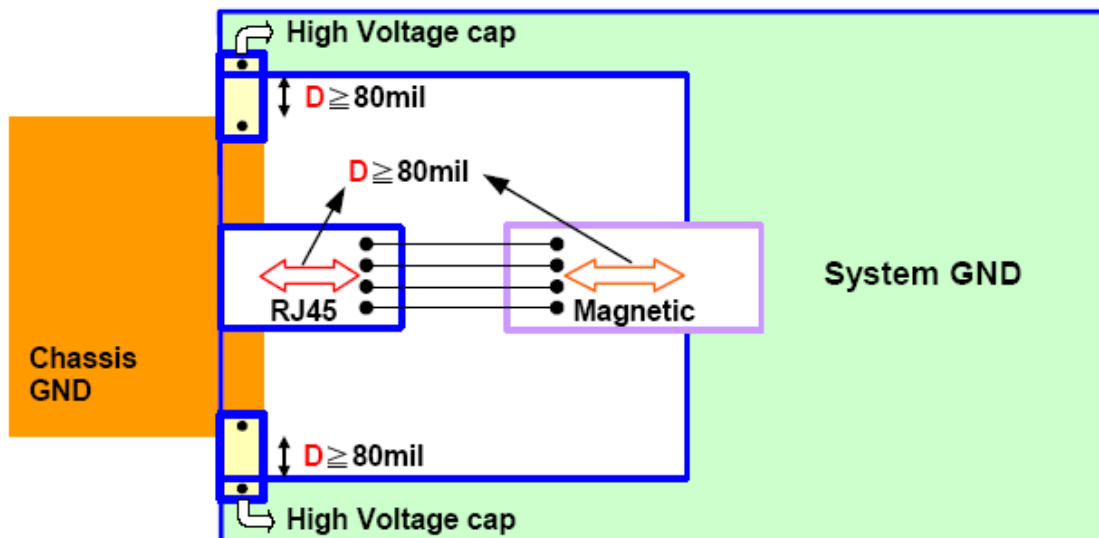
W2: The distance between MDI signal and noisy power /signal should be far enough, ex: 30mils.

Do not use via on the traces of MDI+/-, because via will downgrade the quality of signals.

- **Avoid the interference among digital signals (such as Clocks or GMII/RGMII signal traces), analog signals (such as Tx+/-, Rx+/-) and power lines. Never run noisy digital signals in parallel with TX+/- and RX+/-.**
- **The traces of power, ground for de-coupling capacitor should be shorter and wider. If vias are inevitable on the trace for de-coupling capacitor, try to enlarge the diameter of these vias.**
- **The signal trace length difference between Tx+ and Tx- (Same as Rx+ and Rx-) should be kept as small as possible, better within 300 mils.**
- **Ferrite Beads should be as close to IC pins and at the spec.**
For signal path: $>100\Omega @100\text{MHz}$,
For power path: $>75\Omega @100\text{MHz}$, $< 0.05\Omega @\text{DC}$
- **The spec of crystal accuracy should be under 50ppm deviation, please refer to the attached crystal's spec. Capacitance attached to X1 and X2 should be close to 30pF.**
- **RSET of IP1001 (pin 17) should be placed as close to IP1001 as possible. Furthermore, it should not be affected by other signals such as TX+/-, RX+/- and clock signal traces.**

6 ESD protection

- For ESD protection, we suggest to keep a distance at least 80 mil for good isolation between the chassis GND and the signal GND to avoid ESD energy jumping by traces nearby IC. (See the diagram below)



D is isolation area between System GND and Chassis GND.
D is isolation area between TX/RX and Chassis GND.

7 EMI Supression

- **If possible, shield the high speed signal with GND trace. This will help reduce EMI effect.**
- **NEVER run any power plane and unnecessary signals near to the crystal components, especially the reference clock source (pin X1). This will worsen the clock jitter and EMI problems.**
- **NEVER run any power plane and unnecessary signals under the I/O connectors(such as RJ45). This will couple undesired noises onto cables or emit RF signal into the air, causing EMI issue.**