

Purpose:

This application note provides some useful configurations such as LED mode setting, regulator control & power source, hardware setting and power consumption... etc.

IP1001 LF Interface Diagram

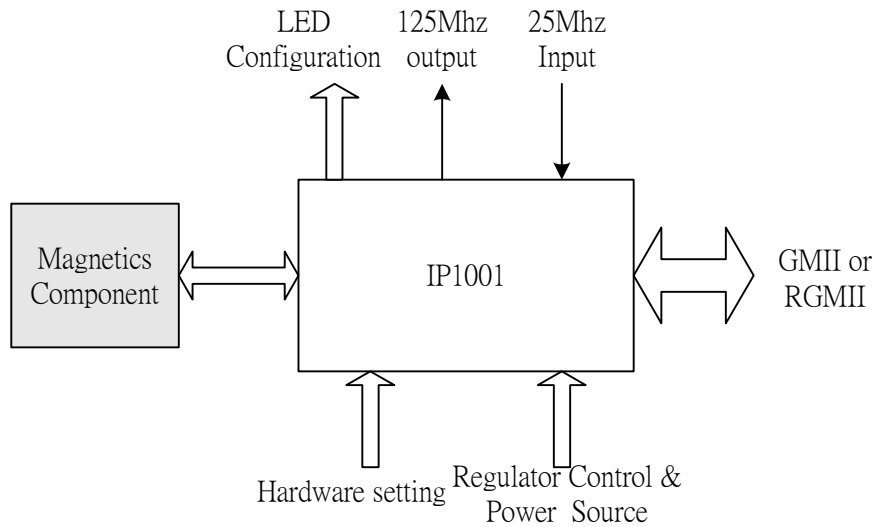


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1 LED configuration

IP1001 provides 3 LED pins (LED0~ LED2) and four LED display modes (mode0~ mode3). User can select one of four LED modes by configuring LED_MODE1 and LED_MODE0. LED_MODE1 and LED_MODE0 are defined in register 16[15:14]. Pin 55 LED_MODE0 defines the default value of register 16[14].

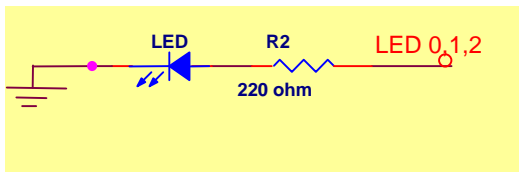
LED mode 1



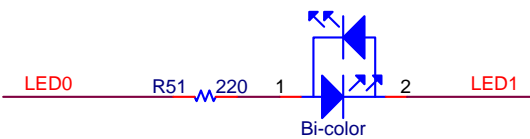
LED mode 0



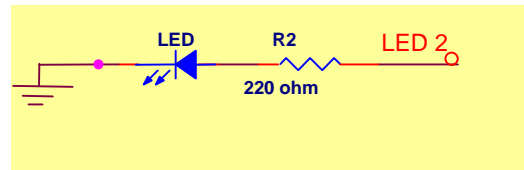
1.1 LED Mode 0 & mode 2



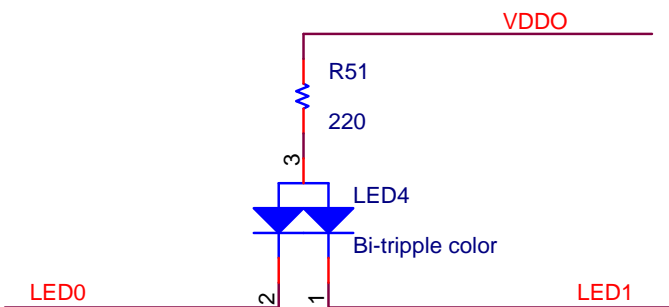
1.2 LED Mode 1



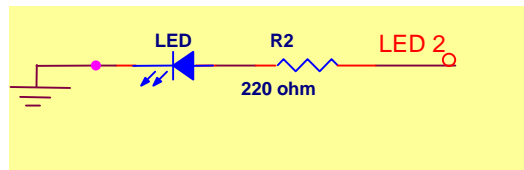
Bi-color LED configuration



1.3 LED Mode 3



Bi-tripple color LED configuration



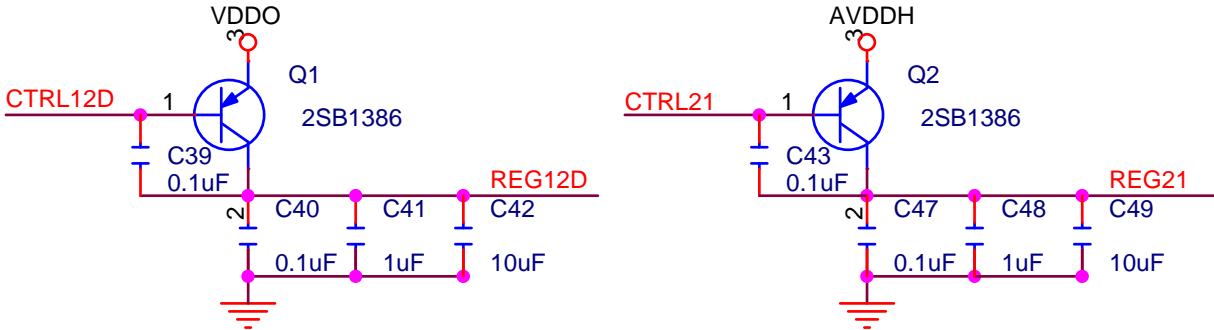


IP1001 LF APPLICATION NOTE

Pin no.	Label	Type	Description					
55	LED_MODE0	LI/O	LED Mode Selection (MODE0~MODE3) User can select one of four LED modes, mode0 ~ mode3 by programming register 16[15:14]. The default value of register 16[15] is "0". The default value of register 16[14] is defined by this pin. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>LED_MODE1</td> <td>LED_MODE0</td> </tr> <tr> <td>Register16 [15]</td> <td>Register16 [14] / pin 55</td> </tr> </table>		LED_MODE1	LED_MODE0	Register16 [15]	Register16 [14] / pin 55
LED_MODE1	LED_MODE0							
Register16 [15]	Register16 [14] / pin 55							
15,14,13	LED2, LED1, LED0	IPH/O, LI/O	LED output pins 0,1,2					
			Mode0	Mode1	Mode2	Mode3		
			00	01	10	11		
			LED_Mode1, LED_Mode0					
LED0	10/100M Link/Act 0: link off 1: 10/100M link on Flash: TX or RX	Bi-color mode {LED0, LED1}= 10= 1G Link; 01=10/100M Link;	1G Link/Act 0: link off 1: Giga link on Flash: TX or RX	Bi-triple-color mode {LED0, LED1}= 10= 1G Link; 01= 100M Link				
LED1	100M Link/Act 0: link off 1: 100M link on Flash: TX or RX	00= link off 11= link off	100M Link/Act 0: link off 1: 100M link on Flash: TX or RX	00= 10M Link; 11= link off				
LED2	1G Link/Act 0: link off 1: Giga link on Flash: TX or RX	Act 0: link off or idle 1: TX or RX	10M Link/Act 0: link off 1: 10M link on Flash: TX or RX	Link/ Act 0: link off 1: 10/100M/giga link on Flash: TX or RX				

2 Regulator Control & Power Supply

2.1 Regulator control



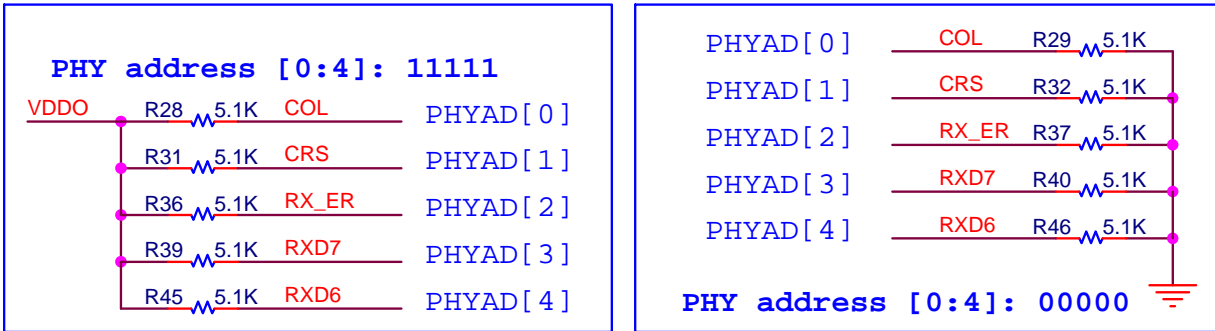
Note: REG12D=1.2V for DVDD only
REG21=2.15V for AVDD only

2.2 Power Supply Table

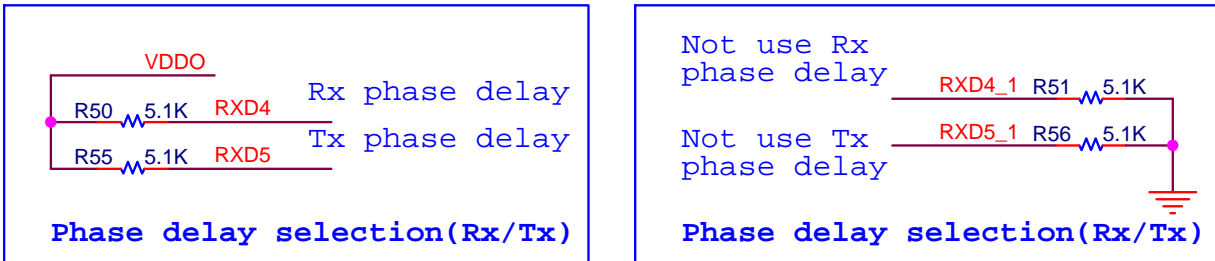
	GMII/MII		RGMII		Note
VDDO	3.3V		2.5V		3.3V or 2.5V supplied by system
AVDDH	3.3V		2.5V		3.3V or 2.5V supplied by system
AVDD	(1)	(2)	(1)	(2)	(1) When AVDD=1.8V supplied by system and DVDD=1.2V supplied by system. (2) When AVDD=2.1V is generated by controlling PNP transistor through CTRL21 and DVDD=1.2V is generated by controlling PNP transistor through CTRL12D.
DVDD					
Center tap of the transformer	2.5V or 2.1V		2.5V or 2.1V		Center tap=2.5V or 2.1V depending on whether CTRL21 is used to generate 2.1V.

3 Hardware setting

3.1 PHY address setting



3.2 Phase delay setting



3.3 Interface selection

GMII/MII interface



RGMII interface



4 Dealing with unused pin

Do not leave unused input pin floating unless there is an internal pull-up or pull-low resistor in the chip. Use a resistor, ranging from 1K ~ 4.7K, to force the input to a fixed state.



5 Power Consumption

5.1 RGMII mode

Link Mode	VDDO	DVDD	AVDDH	AVDD	CT (2.5V)	Total watt
Actual Voltage	2.5V	1.2V	2.5V	1.8V	2.5V	
1000M(TX &RX)	26mA	294mA	62mA	84mA	179mA	1.1665W
100M(TX &RX)	24mA	57mA	49mA	36mA	47mA	0.4282W
10M (TX&RX)	20mA	8mA	45mA	24mA	54mA	0.3503W
No link (APS mode)	18mA	4mA	44mA	20mA	11mA	0.2233W

5.2 GMII mode

Link Mode	VDDO	DVDD	AVDDH	AVDD	CT (2.5V)	Total watt
Actual Voltage	3.3V	1.2V	3.3V	1.8V	2.5V	
1000M (TX &RX)	55mA	295mA	69mA	84mA	179mA	1.3553W
100M(TX&RX)	53mA	58mA	55mA	35mA	46mA	0.5875W
10M(TX&RX)	44mA	8mA	52mA	24mA	54mA	0.5046W
No link (APS mode)	41mA	4mA	50mA	20mA	11mA	0.3686W

6 Magnetic information

- IP1001 require that MDI+/- turn ration 1:1/1:1 with 4 channels. We list the manufacturers as below for reference. Magnetic that supports Auto-MDIX function is recommended for better EMI performance.

Vendor	Part number
FUN-JIN	GT24-03S
Bothhand	24HST1041A, GST5009
Pulse	H5004, H5091NL
TAIMAG	IH-002



7 EMI Suppression

- Use slower Slew Rate setting defined in Register 20[1:0] to improve EMI performance as long as the GMII/RGMII function is ok. Also keep the trace of RGMII or GMII as short as possible. Adjusting the slew rate will affect RGMII/GMII/MII characteristics, so you should measure the interface AC characteristics to ensure the design still meet the interface spec.

MII Register	Name	Description	Type	HW Reset	SW Reset
20[1:0]	SR_V/ SR_FAST	Slew rate control parameters 00: slew rate = Slowest 01: slew rate = Slow 10: slew rate = Medium 11: slew rate = Fast	RW	11	NA

- Use the lower limit of the supply voltage to reduce the power consumption and improve the EMI performance.
- If possible, shield the high-speed (over 25MHz signal, MDI differential and clock signals, for example) signal with GND. It is helpful to reduce EMI effect.
- NEVER run any power plane and unnecessary signals near the crystal components, especially the reference clock source (pin X1). This will worsen the clock jitter and EMI problems.
- NEVER run any power plane and unnecessary signals under the I/O connectors (such as RJ45). This will couple undesired noises onto cables and cause EMI issues.
- In a 4 layer PCB design, place IP1001 on the component side (layer-1) and keep layer-2 a complete ground plane.

8 Relationship among Clock, Power Supply and Reset

- Please refer to the data sheet



9 IEEE802.3 TX template measurement

Mode		Function
10M	Link pulse	Write Reg. 0x14 Data=0x056B (Disable Auto MDIX and APS) Write Reg. 0x00 Data=0x0100 (Force 10M) Measure channel A of MDI differential pair.
	Random pattern for Differential Voltage, TP-IDLE, Jitter	Write Reg. 0x14 Data=0x056B (Disable Auto MDIX and APS) Write Reg. 0x00 Data=0x0100 (Force 10M) Link to 10M hub (connect the channel B of DUT to the TX path of 10M hub). MAC device send out random data (1514Bytes) pattern. Measure channel A of MDI differential pair.
	All one pattern for Harmonic	Write Reg. 0x14 Data=0x056B (Disable Auto MDIX and APS) Write Reg. 0x00 Data=0x0100 (Force 10M) Link to 10M hub (connect the channel B of DUT to the TX path of 10M hub). MAC device send out all one data (1514Bytes) pattern. Measure channel A of MDI differential pair.
100M	MLT-3	Write Reg. 0x14 Data=0x056B (Disable Auto MDIX and APS) Write Reg. 0x00 Data=0x2100 (Force 100M) Measure channel A of MDI differential pair.
1000M	Test mode 1	Write Reg. 0x09 Data=0x2700 Measure channels A, B, C and D of MDI differential pair individually.
	Test mode 4	Write Reg. 0x09 Data=0x8700 Measure channels A, B, C and D of MDI differential pair individually.
Normal mode		Write Reg. 0x09 Data=0x0700 Write Reg. 0x14 Data=0x0D6F (Enable Auto MDIX and APS) Write Reg. 0x00 Data=0x1340 (Restart Auto-Negotiation)