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Test Result Summary

No	Test Item	Test Result	Note
1	MII Register Test & External Loopback Test (UTP Loop Back Test)	Pass	
2	Compatibility under Various Cable Length <ul style="list-style-type: none">● Various SmartBits Modules● PCI Adapter Card● PHY	Pass	
3	UNH-IOL Interoperability Group 1 ~ Group 3	Pass	
4	Plug/unplug cable & Power on/off	Pass	
5	Maximum Packet size of Jumbo Packet	9000 Bytes	
6	IEEE 802.3 waveform Template <ul style="list-style-type: none">● 1000Base-T (Channel A to Channel D)● 100Base-TX (MDI & MDIX)● 10 Base-T(MDI & MDIX)	<ul style="list-style-type: none">● 1000Base-T: Pass● 100Base-TX: Pass● 10Base-T: Pass.	
7	Power Consumption & IC Surface Temperature		
8	Power Supply Range & Operating Temperature Range		



1 MII Register and LoopBack Test

1.1 MII Register Read / Write

Test Program	Read/Wrote MII registers through MII access tool
Result	Pass

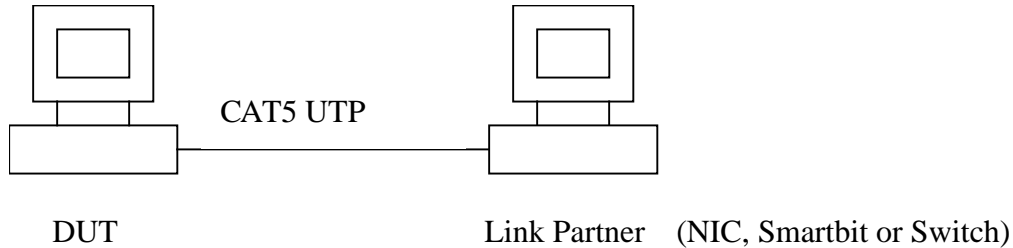
1.2 External Loopback

External loopback connection = TXN -> RXN, TXP -> RXP at RJ-45 phone jack

UTP Connection Test	
Test Program	1nic.exe (TX/RX function)
Test Time	12 hrs
Adapter Card	IP1001 RGMII Riser card
Condition	Compare TX data & RX data
Test Result	Pass (No error was found)

2 Compatibility Test under Various Cable Length

2.1 Environment Setup



Computer	Motherboard			
	Brand	Model	CPU	RAM
DUT board (TC9021+IP1001)	ASUS	P4B266	1.6GHz	256MB
Packet count	10 million packets			
Test program	TSI-TWI for Windows. 1NIC.exe			
Pass Condition	No CRC, no packet loss			

2.2 IP1001 to SmartBits Test Result

Link Partner	Cable Length	Result	Note
Smartbit modules: GX-1420B; LAN-3310A; SX-7405; SX-7410; SX-7410B;	2m; 10m; 20m; 30m; 40m; 50m; 60m; 70m; 80m; 90m; 100m; 110m	Pass	

2.3 IP1001 to Adapter Card Test Result

Link Partner	Cable Length	Result	Note
Adapter card: IP100; IP100A; DFE550TX (DL10050C), D-Link; DFE530TX; (DL10030B); RTL8139C;RTL8139D DM9102AF; Intel Pro100S; 3COM 3C920	2m; 10m; 20m; 30m; 40m; 50m; 60m; 70m; 80m; 90m; 100m; 110m	Pass	



2.4 IP1001 to Switch Test Result

Link Partner	Cable Length	Result	Note
IP178A IP178C IP175A IP175C KS8995 AT8989 ADM6999 RTL8305SB	2m; 10m; 20m; 30m; 40m; 50m; 60m; 70m; 80m; 90m; 100m; 110m	Pass	

2.5 IP1001 to Various PHYs Test Result

Link Partner	Cable Length	Result	Note
VT6508X1 Marvell 88E1040 Marvell 88E1040T CIS8204X CIS8201 BCM5404	2m; 10m; 20m; 30m; 40m; 50m; 60m; 70m; 80m; 90m; 100m; 110m	Pass	



3 UNH-IOL Interoperability test

3.1 UNH-IOL Interoperability with Various PHY

Item	PHY	Manufacturer	PASS/FAIL	Note
1	BCM5400	SPIRENT Smartbits-2000 GX-1420B	PASS	
2	BCM5401	SPIRENT Smartbits-6000 LAN-3310A	PASS	
3	BCM5401	3COM 3C16468	PASS	
4	BCM5404	GIGA-MAC TC9208M	PASS	
5	CIS 8204X + CIS 8201	GIGA-MAC TC9205M	PASS	
6	M88E1040T	SureCOM EP-805CG-S	PASS	
7	M88E6050	Marvell PHY	PASS	
8	LXT970QC	SPIRENT Smartbits-2000 SX-7410B	PASS	
9	LXT970QC	SPIRENT Smartbits-2000 SX-7410 (LevelOne PHY Date Code 9749 DSQ8)	PASS	
10	DP83223V	SPIRENT Smartbits-2000 SX-7405 (NS PHY ET9717AFC4)	PASS	
11	KS8995	D-Link DES-10050 Kendin PHY	PASS	
12	RTL 8305SB	Realtek PHY	PASS	
13	Level One 974	SPIRENT Smartbits-6000 LAN-3100A	PASS	



3.2 Test Items

No.	Test Item				Status	--	Note
UNH-IOL Testing							
Physical Layer Interoperability Test Suite							
1	GROUP 1: POINT-TO-POINT INTEROPERABILITY				--	--	--
1.1	Link Speed Detection				PASS		IEEE802.3-2000 Clause 28.2.3.3
	Item	Description		--			
	1.1	Power on DUT first, and power on Link Partner later.		PASS			
	1.2	Power on Link Partner first, and power on DUT later.		PASS			
	1.3	Power on DUT and Link Partner at the same time.		PASS			
	2.1	Establish a valid Highest Common Denominator (HCD) link		PASS			
1.2	Packet Error Ratio Estimation				PASS		
IEEE802.3-2000 Clause 28 Auto-Negotiation Management System Test Suite							
3	GROUP 1: ABILITY ADVERTISEMENT				--	--	--
3.1	Auto-Negotiation on/off				PASS		IEEE802.3-2000 Clause 28 Auto-Negotiation Management System Test Suite
3.2	Base Page Technology Ability Field				PASS		
3.3	1000BASE-T Abilities				PASS		
4	GROUP 2: PRIORITY RESOLUTION						
4.1	Speed Resolution and Verification				PASS		
	Item	DUT (IP1001) Automatic MDI Crossover	Link Partner Automatic MDI Crossover	A, B channel MDI or MDI-X	C, D channel MDI or MDI-X	--	
	1.1	Enable	Enable	MDI	MDI	PASS	
	1.2			MDI-X	MDI	PASS	
	1.3			MDI	MDI-X	PASS	
	1.4			MDI-X	MDI-X	PASS	
	2.1	Disable	Disable	MDI	MDI	PASS	
	2.2			MDI-X	MDI	PASS	
	2.3			MDI	MDI-X	PASS	
	2.4			MDI-X	MDI-X	PASS	
	3.1	Enable	Disable	MDI	MDI	PASS	
	3.2			MDI-X	MDI	PASS	
	3.3			MDI	MDI-X	PASS	
	3.4			MDI-X	MDI-X	PASS	
	4.1	Disable	Enable	MDI	MDI	PASS	

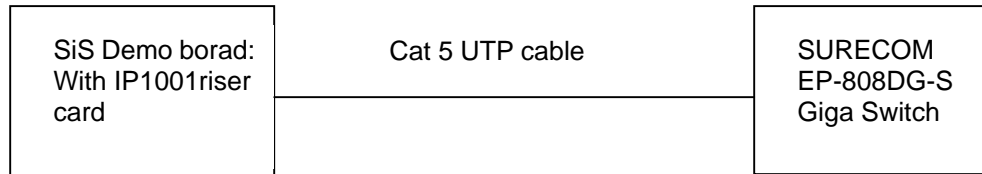


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	4.2			MDI-X	MDI	PASS		
	4.3			MDI	MDI-X	PASS		
	4.4			MDI-X	MDI-X	PASS		
4.2	Duplex Resolution and Verification					PASS		
4.3	Pause Mode Resolution					PASS		
4.4	1000BASE-T Master-Slave Resolution					PASS		
5	GROUP 3: Parallel Detection					--		
5.1	Parallel Detection of 10BASE-T Devices					PASS		
	Item	DUT (IP1001) Automatic MDI Crossover	Link Partner Automatic MDI Crossover	A, B channel MDI or MDI-X		--		
	1.1	Enable	Enable	MDI		PASS		
	1.2			MDI-X		PASS		
	2.1	Disable	Disable	MDI		PASS		
	2.2			MDI-X		PASS		
	3.1	Enable	Disable	MDI		PASS		
	3.2			MDI-X		PASS		
	4.1	Disable	Enable	MDI		PASS		
	4.2			MDI-X		PASS		
5.2	Parallel Detection of 100BASE-TX Devices					PASS		
	Item	DUT (IP1001) Automatic MDI Crossover	Link Partner Automatic MDI Crossover	A, B channel MDI or MDI-X		--		
	1.1	Enable	Enable	MDI		PASS		
	1.2			MDI-X		PASS		
	2.1	Disable	Disable	MDI		PASS		
	2.2			MDI-X		PASS		
	3.1	Enable	Disable	MDI		PASS		
	3.2			MDI-X		PASS		
	4.1	Disable	Enable	MDI		PASS		
	4.2			MDI-X		PASS		

4 Cable plug/unplug test and Power on/off Test

4.1 Test Setup



4.2 Purpose

To test whether the DSP part can settle down at a stable link status whenever the cable is plugged to the phone jack or the power is switched on.

4.3 Procedure

- (1) Plug/unplug cable at the IP1001 riser card end for 100 times. Watch whether both ends link at the same speed.
- (2) Power on/off the switch for 100 times and watch whether both ends link at the same speed.

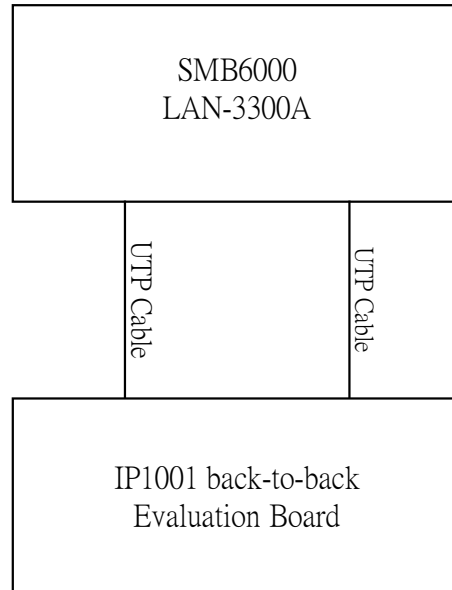
4.4 Test Result

No abnormal symptom was found.

5 Maximum Size of Jumbo Packet

5.1 Test Seup:

1. The seup is shown below.
2. Send 100K packets to each other through Smartbits and back-to-back evaluation Board.



5.2 Test result:

IP1001 can handle 9000 Bytes packet size.



6 IEEE 802.3 Waveform Template Test

6.1 1000BASE-T Test Result (Specification: Section 40.6.1.2) Channel A

Measured Item	Specification	Measured Value	Measured Result
(1) 1000Base-T Differential output template point A	Within Waveform Limit	Within Waveform Limit	Pass
(2) 1000Base-T Differential output template point B	Within Waveform Limit	Within Waveform Limit	Pass
(3) 1000Base-T Differential output template point C	Within Waveform Limit	Within Waveform Limit	Pass
(4) 1000Base-T Differential output template point D	Within Waveform Limit	Within Waveform Limit	Pass
(5) 1000Base-T Differential output template point F	Within Waveform Limit	Within Waveform Limit	Pass
(6) 1000Base-T Differential output template point H	Within Waveform Limit	Within Waveform Limit	Pass
(7) 1000Base-T Differential output voltage point A	670 mV ~ 820 mV	707.8 mV	Pass
(8) 1000Base-T Differential output voltage point B	670 mV ~ 820 mV, Difference A & B <1 %	708.3 mV 0.073 %	Pass
(9) 1000Base-T Differential output voltage point C	Difference between C & 0.5 times the average of A and B <2 %	354.4 mV 0.111 %	Pass
(10) 1000Base-T Differential output voltage point D	Difference between D & 0.5 times the average of A and B <2 %	357.7 mV 1.018 %	Pass
(11) 1000Base-T Maximum output droop point G	Ratio of the voltage at point G to the voltage at point F > 73.1 %	96.3 %	Pass
(12) 1000Base-T Maximum output droop point J	Ratio of the voltage at point J to the voltage at point H > 73.1 %	96 %	Pass

6.2 1000BASE-T Test Result (Specification: Section 40.6.1.2) Channel B

Measured Item	Specification	Measured Value	Measured Result
(13) 1000Base-T Differential output template point A	Within Waveform Limit	Within Waveform Limit	Pass
(14) 1000Base-T Differential output template point B	Within Waveform Limit	Within Waveform Limit	Pass
(15) 1000Base-T Differential output	Within Waveform Limit	Within Waveform Limit	Pass



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template point C			
(16)1000Base-T Differential output template point D	Within Waveform Limit	Within Waveform Limit	Pass
(17)1000Base-T Differential output template point F	Within Waveform Limit	Within Waveform Limit	Pass
(18)1000Base-T Differential output template point H	Within Waveform Limit	Within Waveform Limit	Pass
(19)1000Base-T Differential output voltage point A	670 mV ~ 820 mV	700.3 mV	Pass
(20)1000Base-T Differential output voltage point B	670 mV ~ 820 mV, Difference A & B <1 %	703.1 mV 0.391 %	Pass
(21)1000Base-T Differential output voltage point C	Difference between C & 0.5 times the average of A and B <2 %	349.1 mV 0.511 %	Pass
(22) 1000Base-T Differential output voltage point D	Difference between D & 0.5 times the average of A and B <2 %	350.7 mV 0.048 %	Pass
(23) 1000Base-T Maximum output droop point G	Ratio of the voltage at point G to the voltage at point F > 73.1 %	96.3 %	Pass
(24) 1000Base-T Maximum output droop point J	Ratio of the voltage at point J to the voltage at point H > 73.1 %	96 %	Pass

6.3 1000BASE-T Test Result (Specification: Section 40.6.1.2) Channel C

Measured Item	Specification	Measured Value	Measured Result
(25)1000Base-T Differential output template point A	Within Waveform Limit	Within Waveform Limit	Pass
(26)1000Base-T Differential output template point B	Within Waveform Limit	Within Waveform Limit	Pass
(27)1000Base-T Differential output template point C	Within Waveform Limit	Within Waveform Limit	Pass
(28)1000Base-T Differential output template point D	Within Waveform Limit	Within Waveform Limit	Pass
(29)1000Base-T Differential output template point F	Within Waveform Limit	Within Waveform Limit	Pass
(30)1000Base-T Differential output template point H	Within Waveform Limit	Within Waveform Limit	Pass
(31)1000Base-T Differential output voltage point A	670 mV ~ 820 mV	689.3 mV	Pass
(32)1000Base-T Differential output voltage point B	670 mV ~ 820 mV, Difference A & B <1 %	690.5 mV 0.178 %	Pass
(33)1000Base-T Differential output voltage point C	Difference between C & 0.5 times the average of A and B <2 %	345 mV 0.016 %	Pass



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(34) 1000Base-T Differential output voltage point D	Difference between D & 0.5 times the average of A and B <2 %	345.3 mV 0.092 %	Pass
(35) 1000Base-T Maximum output droop point G	Ratio of the voltage at point G to the voltage at point F > 73.1 %	96.2 %	Pass
(36) 1000Base-T Maximum output droop point J	Ratio of the voltage at point J to the voltage at point H > 73.1 %	95.9 %	Pass

6.4 1000BASE-T Test Result (Specification: Section 40.6.1.2) Channel D

Measured Item	Specification	Measured Value	Measured Result
(37) 1000Base-T Differential output template point A	Within Waveform Limit	Within Waveform Limit	Pass
(38) 1000Base-T Differential output template point B	Within Waveform Limit	Within Waveform Limit	Pass
(39) 1000Base-T Differential output template point C	Within Waveform Limit	Within Waveform Limit	Pass
(40) 1000Base-T Differential output template point D	Within Waveform Limit	Within Waveform Limit	Pass
(41) 1000Base-T Differential output template point F	Within Waveform Limit	Within Waveform Limit	Pass
(42) 1000Base-T Differential output template point H	Within Waveform Limit	Within Waveform Limit	Pass
(43) 1000Base-T Differential output voltage point A	670 mV ~ 820 mV	704 mV	Pass
(44) 1000Base-T Differential output voltage point B	670 mV ~ 820 mV, Difference A & B <1 %	705 mV 0.133 %	Pass
(45) 1000Base-T Differential output voltage point C	Difference between C & 0.5 times the average of A and B <2 %	352 mV 0.086 %	Pass
(46) 1000Base-T Differential output voltage point D	Difference between D & 0.5 times the average of A and B <2 %	351.7 mV 0.154 %	Pass
(47) 1000Base-T Maximum output droop point G	Ratio of the voltage at point G to the voltage at point F > 73.1 %	96.3 %	Pass
(48) 1000Base-T Maximum output droop point J	Ratio of the voltage at point J to the voltage at point H > 73.1 %	98 %	Pass



6.5 100BASE-T Test Result (Specification: ANSI X3.263-1995) MDI TX

Measured Item	Specification	Measured Value	Measured Result
(1) Annex J AOI Template (Transmit Eye Diagram)	Within Waveform Limit	Within Waveform Limit	Pass
(2) Section 9.1.2.2: Differential Output Voltage	+Vout: 0.95V~1.05V -Vout: -0.95V~-1.05V	+Vout: 996.2 mV -Vout: -993.1 mV	Pass
(3) Section 9.1.4: Signal Amplitude Symmetry	0.98~1.02(+Vout/-Vout)	1.003	Pass
(4) Section 9.1.6: Rise time	3ns~5ns	+Ve=> 3.82 ns -Ve=> 3.85 ns	Pass
(5) Section 9.1.6: Fall time	3ns~5ns	+Ve=> 4.04 ns -Ve=> 4.04 ns	Pass
(6) Section 9.1.6: Rise Fall Symmetry	< 500ps	+Ve=> 248 ps -Ve=> 125 ps	Pass
(7) Section 9.1.3: Waveform Overshoot	< 5%	+Ve=> 1.65 % -Ve=> 0 %	Pass
(8) Section 9.1.9: Transmit Jitter	< 1.4ns	+Ve=> 490 ps -Ve=> 450 ps	Pass
(9) Section 9.1.8: Distortion (Duty Cycle)	< 500ps(+/-250ps)	250 ps	Pass

6.6 100BASE-T Test Result (Specification: ANSI X3.263-1995) MDIX TX

Measured Item	Specification	Measured Value	Measured Result
(10) Annex J AOI Template (Transmit Eye Diagram)	Within Waveform Limit	Within Waveform Limit	Pass
(11) Section 9.1.2.2: Differential Output Voltage	+Vout: 0.95V~1.05V -Vout: -0.95V~-1.05V	+Vout: 970.1 mV -Vout: -968.6 mV	Pass
(12) Section 9.1.4: Signal Amplitude Symmetry	0.98~1.02(+Vout/-Vout)	1.002	Pass
(13) Section 9.1.6: Rise time	3ns~5ns	+Ve=> 4.07 ns -Ve=> 4.04 ns	Pass
(14) Section 9.1.6: Fall time	3ns~5ns	+Ve=> 4.25 ns -Ve=> 4.15 ns	Pass
(15) Section 9.1.6: Rise Fall Symmetry	< 500ps	+Ve=> 272 ps -Ve=> 135 ps	Pass
(16) Section 9.1.3: Waveform Overshoot	< 5%	+Ve=> 1.42 % -Ve=> 0 %	Pass
(17) Section 9.1.9: Transmit Jitter	< 1.4ns	+Ve=> 500 ps -Ve=> 460 ps	Pass
(18) Section 9.1.8: Distortion (Duty Cycle)	< 500ps(+/-250ps)	200 ps	Pass



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6.7 10BASE-T Test Result (Specification: IEEE Std802.3 Section 14.3 & B 4.3.3) MDI -TX

Measure Item	Specification	Measured value	Measure Result
(1) Section 14.3.1.2.1 : MAU Internal & Internal Inverted Template	Within Waveform limit	Within Waveform Limit	Pass
(2) Section 14.3.1.2.1 : Link Pulse without TPM Load1 & 2 & 3	Within Waveform limit	Within Waveform Limit	Pass
(3) Section 14.3.1.2.1 : Link Pulse with TPM Load 1 & 2 & 3	Within Waveform limit	Within Waveform Limit	Pass
(4) Section 14.3.1.2.1 : TP Idle Pulse without TPM Load 1 & 2 & 3	Within Waveform limit	Within Waveform Limit	Pass
(5) Section 14.3.1.2.1 : TP Idle Pulse with TPM Load 1 & 2 & 3	Within Waveform limit	Within Waveform Limit	Pass
(6) Section 14.3.1.2.1 : Differential Output Voltage	+Vdif: 2.2V~2.8V -Vdif: -2.2V~-2.8V	+Vdif: 2.64 V -Vdif: -2.68 V	Pass
(7) Section 14.3.1.2.1 : Harmonics of all ones	< -27dB (Fundamental to each Harmonic)	37.1 dB	Pass
(8) Section 14.3.1.2.3 : Output Timing Jitter with cable(TPM)	< +/- 8ns	1.3 ns	Pass
(9) Section 14.3.1.2.3 : Output Timing Jitter without cable(TPM)	< +/- 8ns	300 ps	Pass

6.8 10BASE-T Test Result (Specification: IEEE Std802.3 Section 14.3 & B 4.3.3) MDIX-TX

Measure Item	Specification	Measure Value	Measure Result
(10)Section 14.3.1.2.1 : MAU Internal & Internal Inverted Template	Within Waveform limit	Within Waveform Limit	Pass
(11)Section 14.3.1.2.1 : Link Pulse without TPM Load1 & 2 & 3	Within Waveform limit	Within Waveform Limit	Pass
(12)Section 14.3.1.2.1 : Link Pulse with TPM Load 1 & 2 & 3	Within Waveform limit	Within Waveform Limit	Pass
(13)Section 14.3.1.2.1 : TP Idle Pulse without TPM Load 1 & 2 & 3	Within Waveform limit	Within Waveform Limit	Pass
(14)Section 14.3.1.2.1 : TP Idle Pulse with TPM Load 1 & 2 & 3	Within Waveform limit	Within Waveform Limit	Pass
(15)Section 14.3.1.2.1 : Differential Output Voltage	+Vdif: 2.2V~2.8V -Vdif: -2.2V~-2.8V	+Vdif: 2.6 V -Vdif: -2.6 V	Pass
(16)Section 14.3.1.2.1 : Harmonics of all ones	< -27dB (Fundamental to each Harmonic)	34.2 dB	Pass
(17)Section 14.3.1.2.3 : Output Timing Jitter with cable(TPM)	< +/- 8ns	1.3 ns	Pass
(18)Section 14.3.1.2.3 : Output Timing Jitter without cable(TPM)	< +/- 8ns	300 ps	Pass

Test Software: Tektronix Ethernet Compliance Test Software.



7 Power Consumption and IC Surface Temperature

7.1 Power Consumption

RGMII mode

Link Mode	VDDO	DVDD	AVDDH	AVDD	CT (2.5V)	Total watt
Actual Voltage	2.5V	1.2V	2.5V	1.8V	2.5V	
1000M(TX &RX)	26mA	294mA	62mA	84mA	179mA	1.1665W
100M(TX &RX)	24mA	57mA	49mA	36mA	47mA	0.4282W
10M (TX&RX)	20mA	8mA	45mA	24mA	54mA	0.3503W
No link (APS mode)	18mA	4mA	44mA	20mA	11mA	0.2233W

GMII mode

Link Mode	VDDO	DVDD	AVDDH	AVDD	CT (2.5V)	Total watt
Actual Voltage	3.3V	1.2V	3.3V	1.8V	2.5V	
1000M (TX & RX)	55mA	295mA	69mA	84mA	179mA	1.3553W
100M(TX& RX)	53mA	58mA	55mA	35mA	46mA	0.5875W
10M(TX& RX)	44mA	8mA	52mA	24mA	54mA	0.5046W
No link (APS mode)	41mA	4mA	50mA	20mA	11mA	0.3686W

7.2 IC Surface Temperature Test

Test environment:

IC+ IP1001_64 ACR Demo Board Rev A, 4-layer PCB, size: 11.9 cm x 5 cm.

Power supplied by DC power supply HP E3631A, Agilent E3633A, Agilent E3646A

Test condition: Room temperature= 23 °C, wait for linking and TX/RX 5 minutes.

Test result:

Testing table	Ip1001 Temperature (°C)
HYBER mode	27.3
No link (APS mode)	36.4
No link (Disable APS)	30
Link 10M	33.1
10M TX/RX	36.4
Link 100M	36.3
100M TX/RX	36.4
Link 1000M	54.3
1000M TX/RX	56.8



8 Power Supply Range and Operating Temperature Range Test

8.1 Purpose:

To test whether the RGMII phase delay and the internal circuit can work properly under variable temperature and supply voltage.

8.2 Test Environment:

- (1) Place the RGMII back-to-back verification board to the temperature-controlled oven
- (2) Connect both ends with 120m cable to SmartBits. Sends 100K packets data to each other.
- (3) Pass standard: no CRC error, no packet loss.

8.3 Test Result

Test 1:

- (1) Temperature: High=75°C; Normal:=25°C; Low:=-5°C
- (2) Supply voltage: Center tap=AVDDH=VDDO=2.5V [Normal voltage] or Normal voltage-5% or Normal voltage+5%, AVDD=2.1V, DVDD=1.2V,

Voltage	Temperature	Rx Part Delay	Tx part Delay	Result	Note
-5%	Normal	Delay	No	Pass	
+5%	Normal	Delay	No	Pass	
-5%	High	Delay	No	Pass	
+5%	High	Delay	No	Pass	
-5%	Low	Delay	No	Pass	
+5%	Low	Delay	No	Pass	
-5%	Normal	No	Delay	Pass	
+5%	Normal	No	Delay	Pass	
-5%	High	No	Delay	Pass	
+5%	High	No	Delay	Pass	
-5%	Low	No	Delay	Pass	
+5%	Low	No	Delay	Pass	

Test 2:

- (3) Temperature: High=75°C; Normal:=25°C; Low:=-5°C
- (4) Supply voltage: AVDD=2.1V [Normal voltage] or Normal voltage-5% or Normal voltage+5%, , DVDD=1.2V, Center tap=AVDDH=VDDO=2.5V

Voltage	Temperature	Rx Part Delay	Tx part Delay	Result	Note
-5%	Normal	Delay	No	Pass	
+5%	Normal	Delay	No	Pass	
-5%	High	Delay	No	Pass	
+5%	High	Delay	No	Pass	
-5%	Low	Delay	No	Pass	
+5%	Low	Delay	No	Pass	
-5%	Normal	No	Delay	Pass	
+5%	Normal	No	Delay	Pass	
-5%	High	No	Delay	Pass	
+5%	High	No	Delay	Pass	
-5%	Low	No	Delay	Pass	
+5%	Low	No	Delay	Pass	



Test 3:

(5) Temperature: High=75°C; Normal:=25°C; Low:= -5°C

(6) Supply voltage: DVDD=1.2V [Normal voltage] or Normal voltage-5% or Normal voltage+5%,
AVDD=2.1V, Center tap=AVDDH=VDDO=2.5V

Voltage	Temperature	Rx Part Delay	Tx part Delay	Result	Note
-5%	Normal	Delay	No	Pass	
+5%	Normal	Delay	No	Pass	
-5%	High	Delay	No	Pass	
+5%	High	Delay	No	Pass	
-5%	Low	Delay	No	Pass	
+5%	Low	Delay	No	Pass	
-5%	Normal	No	Delay	Pass	
+5%	Normal	No	Delay	Pass	
-5%	High	No	Delay	Pass	
+5%	High	No	Delay	Pass	
-5%	Low	No	Delay	Pass	
+5%	Low	No	Delay	Pass	