

IP1726+IP108 PCB Layout Guide

1. Introduction

This guide will help one to make good PCB for IP1726+IP108 circuit board.

The goals for this document are to reduce noise and other interference to the chip, and also to prevent the EMI effect of the chip. There are following sections will be covered:

- General layout guideline
- Ground
- Power Supply
- Signal Trace

2. General Layout Guideline

The following recommended steps would help the customer to gain the maximum performance.

The high speed signal trace should be kept away from the board border at least 100mil width.

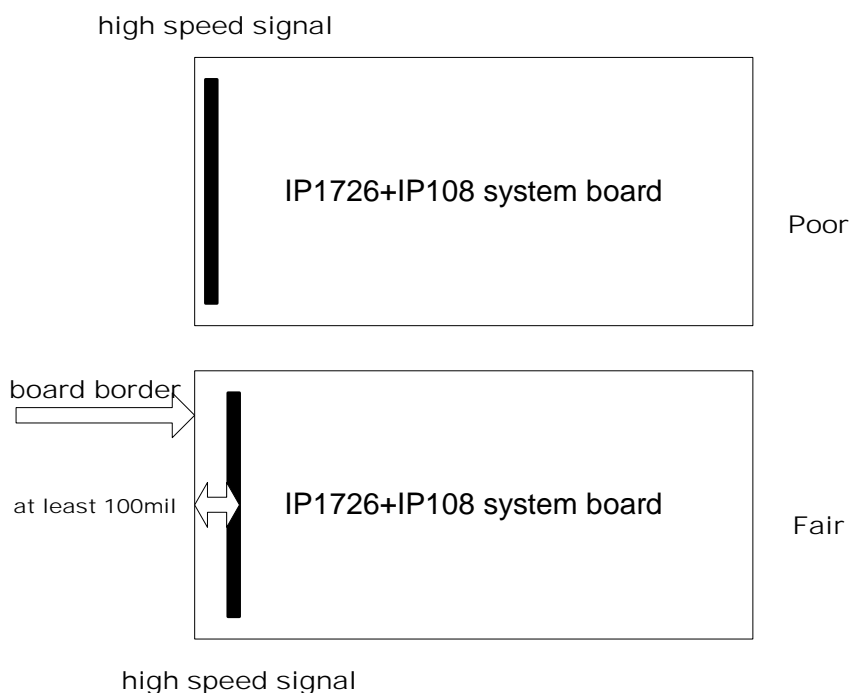


Figure 2.1 Keep the high speed signal away from the border

Utilize the source termination scheme to improve the impedance match and the signal integrity. The termination resistor should be close to the signal output end.

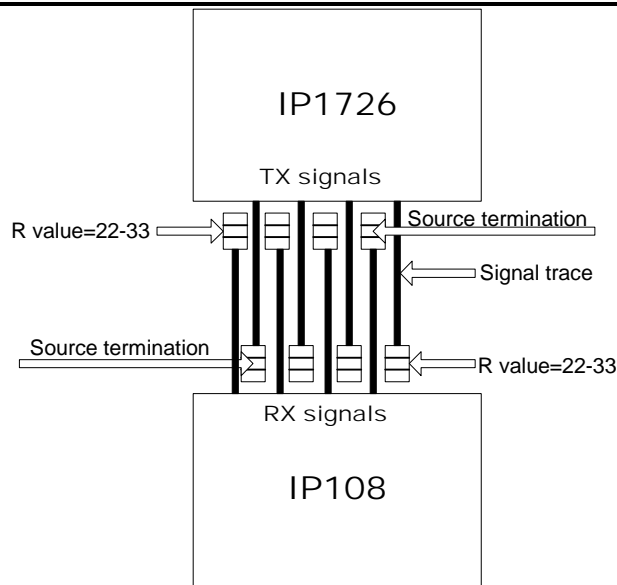


Figure 2.2 Source termination scheme

3. Ground

3.1 Signal Ground

To reduce the electromagnetic radiation and noise coupling, the signal ground plane should be made as an unbroken layer to provide a low impedance for the signal return path.

The following figure shows the incorrect & correct ground plane layout.

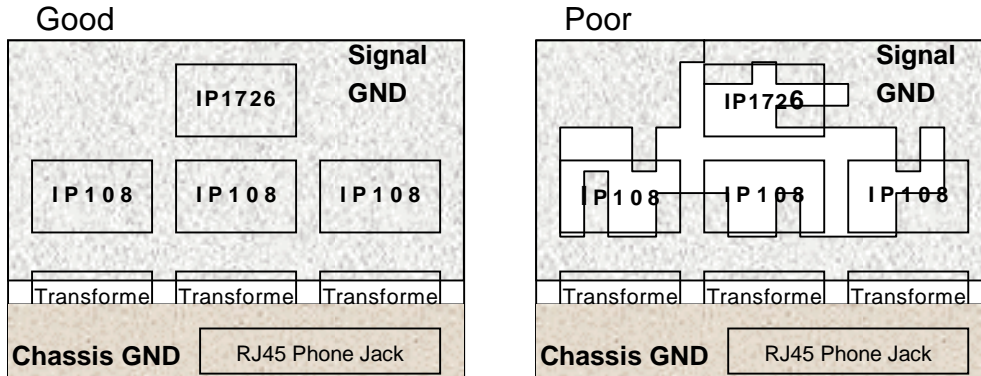


Figure 3.1 The correct & incorrect ground plane

The digital GND and analogue GND should be connected as one large GND plane.

3.2 Chassis Ground

The designer can place a 1nF/2KV capacitor and a large impedance resistor between the Chassis ground and the signal ground. This design can improve the ESD immunity.

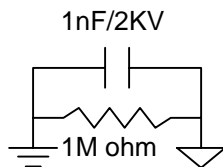


Figure 3.2 Improve the ESD immunity by the extra components

The chassis ground and the signal should be separated by at least 80mils wide.

4. Power

A $0.01 \mu\text{F} \sim 0.1 \mu\text{F}$ capacitor should be placed as close to the power pins as possible ($L < 0.3$ inch) for each VDD and GND pair.

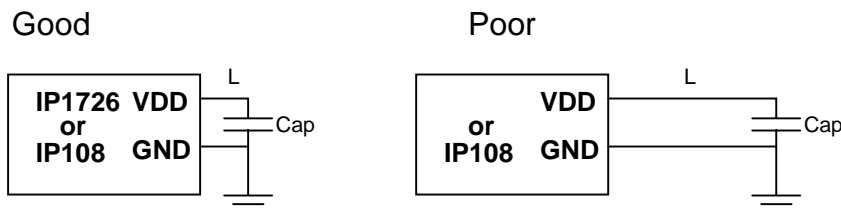
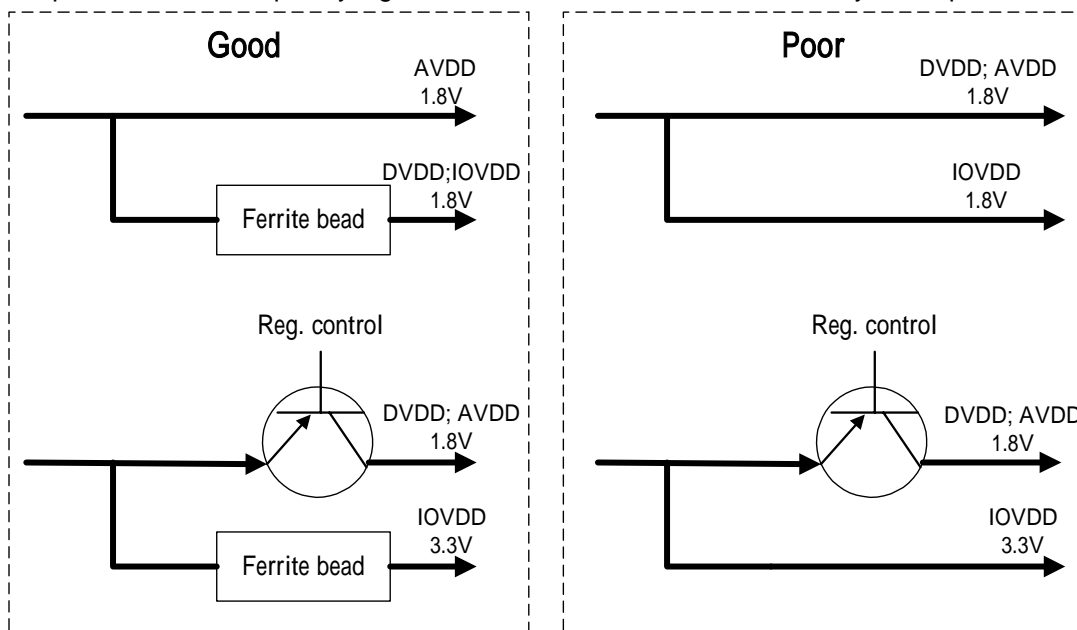


Figure 4.1 Place a decoupling capacitor for each VDD, GND pair

Do not connect the analog power to I/O power directly. Various power sources should be separated by a ferrite BEAD as shown below. The ferrite BEAD should behave like a high impedance at the frequency higher than 100MHz and behave like a very low impedance at the DC.



DVDD: Digital VDD; AVDD: Analog VDD; IOVDD: I/OVDD

Figure 4.2 Power sources separation

Use as many as vias as possible in power connection to keep low impedance when power trace changes layer.

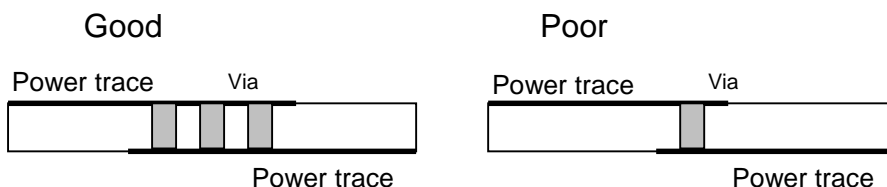


Figure 4.3 Change the layer of the power plane

If a bipolar transistor is used to generate the IP108 1.8V power, the power consumption on the transistor may be as high as 1.45W in the full load case. A solder plate under the transistor for the heat ventilation is necessary. The ventilation area should be at least 70 mm X 70 mm.

5. Signal Trace

5.1 Generic signal trace

Avoid 90° signal tracing.

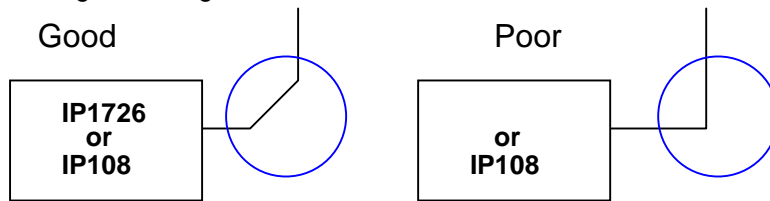
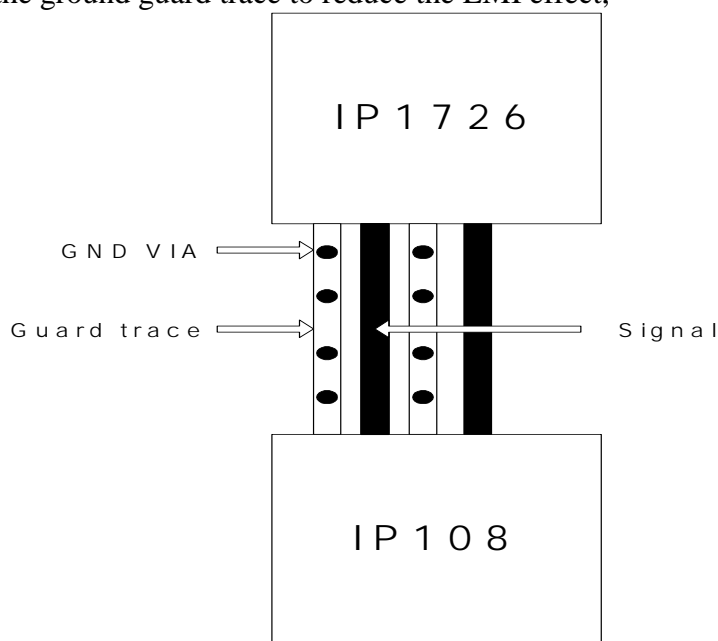


Figure 5.1 Signal trace layout

5.2 SS-SMII

All SS-SMII signal trace should be kept as short as possible. The longer the SS-SMII trace is, the poorer the EMI performance.

Utilize the ground guard trace to reduce the EMI effect,



SS-SMII Interface
Figure 5.2 The SS-SMII layout

5.3 MDC and MDIO recommendation

The MDIO and MDC are routed across every IP108 and IP1726 and likely to be interfered by the high-speed clock, such as TXCLK and RXCLK. It's recommended that the MDC and MDIO should not be parallel to any high-speed clock signal to avoid the interference.

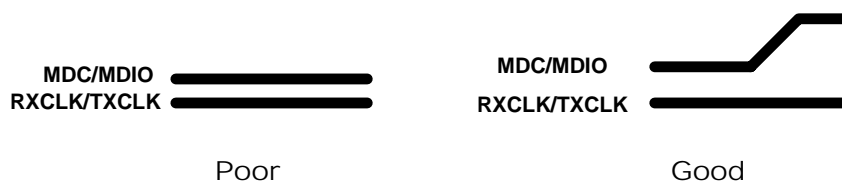
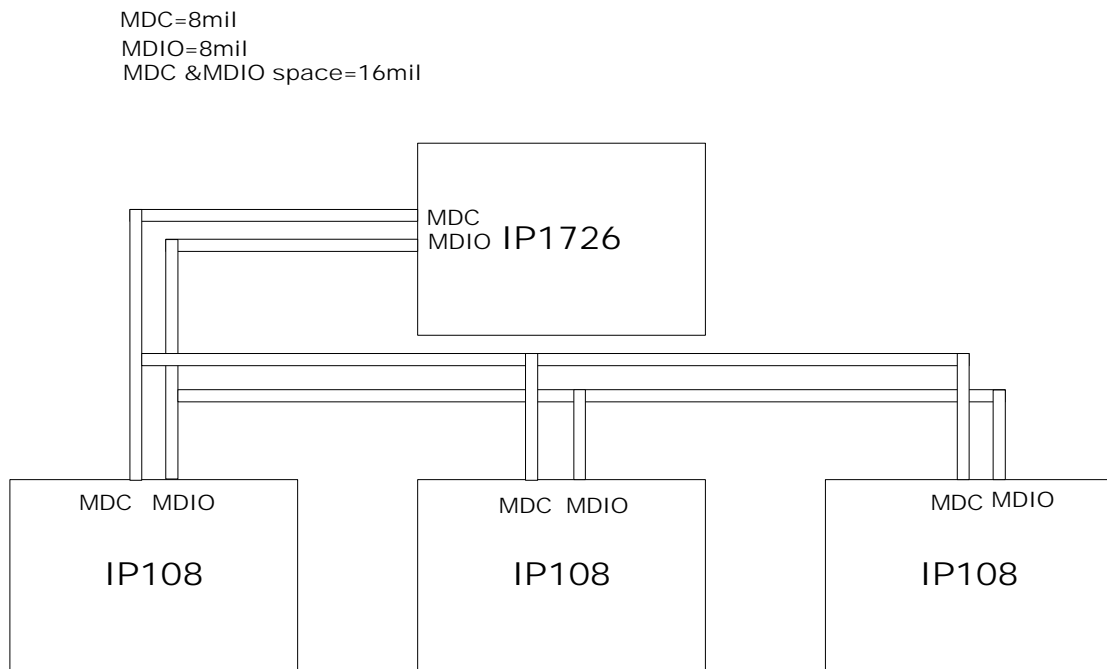


Figure 5.3 Avoid signal interference

In 16 and 24 ports Switch system, the MDC and the MDIO are routed to each PHY device. To achieve the best performance of signal quality, the width and the space for both signals should be routed as the figure shown below



24 ports Switch MDC & MDIO connection

Figure 5.4 MDC and MDIO trace layout

5.4 Transformer and RJ-45 phone jack

The termination resistors should be close to the output of the TD+/- pair of the IP108. It is recommended that the twisted pair trace be routed so that the space between the + signal and the – signal is close to each other. The space between each pair (TX pair or RX pair) is at least 24 mils wide.

In order to keep the impedance match, the via between the secondary winding and the RJ-45 phone jack is not allowed.

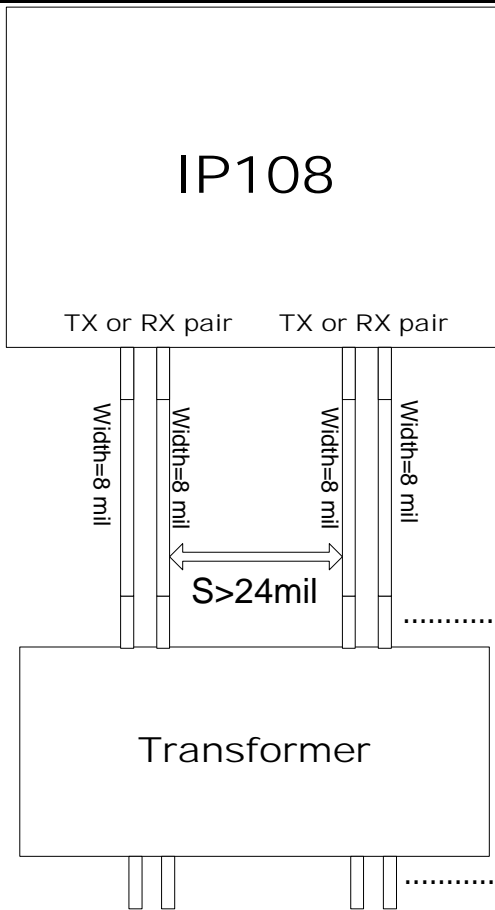


Figure 5.5 Differential pair layout recommendation

The central tap of primary winding of the transformer must be connected to analog 1.8V. A decoupling capacitor(0.01 μ F ~ 0.1 μ F) should be placed close to the primary winding of the transformer.

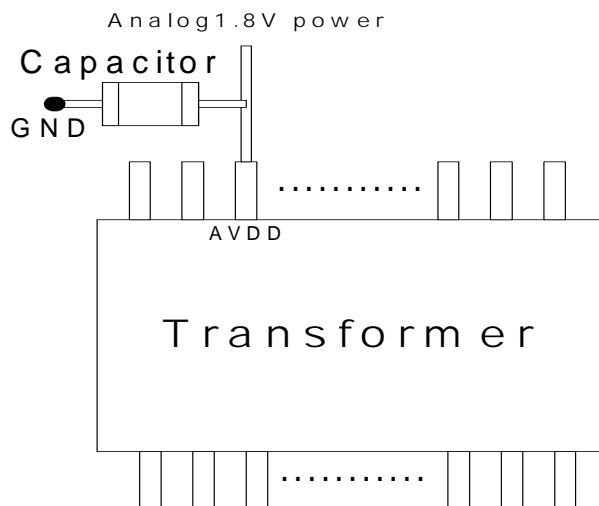


Figure 5.6 The decoupling capacitor at the primary end of the transformer