

IP1726 (1718) + IP108 Application Note

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1 Power consideration

For supporting high port count applications, IPI726+IP108 must use high efficiency power module system, which is preferred for system stability.

1.1 Power consumption in 3.3v/1.8v application

IP108 built in a linear regulator, which provides 1.8v voltage for core and analog circuits. Each IP108 needs an external bipolar transistor.

1.1.1 Power consumption of each components

	IP1726			IP108				PNP	Total power
	VDD33=3.3v	VDD18=1.8v	Power1	VDDIO=3.3v	VDDC=1.8v	AVDD=1.8v	Power2	Power 3	
100M Full	0.06A	0.21A	0.576W	0.02A	0.15A	0.49A	1.218W	0.96W	7.110W
100M Half	0.06A	0.19A	0.540W	0.02A	0.15A	0.49A	1.218W	0.96W	7.074W
100M idle				0.02A	0.15A	0.49A	1.218W	0.96W	6.534W
10M Full	0.06A	0.17A	0.504W	0.02A	0.06A	0.92A	1.83W	1.47W	10.404W
10M Half	0.05A	0.17A	0.471W	0.02A	0.06A	0.92A	1.83W	1.47W	10.371W
10M idle				0.02A	0.06A	0.42A	0.93W	0.72W	4.95W

Note 1: Total power = power1 + 3 X power2 + 3 X power3. Note 2: Idle state is only based on IP108 power

consumption. For example: 24 ports 100 full mode power consumption = 0.576W+1.218WX3+0.96WX3 = 7.110W

1.1.2 Bipolar transistor selection and its layout consideration

The bipolar transistor has to provide about 1A current at worst condition, such as in 10Mbit condition. It is recommended to use ROHM PNP 2SB-1386 to meet the requirement.

For best system reliability, it is recommended that there should be a 10mmx10mm heat sink area on the PCB for the transistor's collector pin. The heat sink area can prevent the PNP transistor from overheat to cause system unstable. Besides, the layout traces of the emitter and collector of the PNP transistor shouldn't be crossed over each other, because it degrades system stability. To enhance system stability, it is recommended that a 0.1uF capacitor should be added between IP108's V_CRTL pin and PNP transistor's collector pin.

1.2 Power consumption in 1.8v application

Both IP1726/1718 and IP108 use a single power of 1.8v voltage. It needs an external switching regulator, such as 34063, to provide the 1.8v power. There is no PNP in this application.

1.2.1 Power consumption of each components

	IP1726		IP108				PNP	Total power
	VDD33=VDD18=1.8v	Power1	VDDIO=1.8v	VDDC=1.8v	AVDD=1.8v	Power2		
100M Full	0.20A	0.360W	0.02A	0.15A	0.49A	1.18W	No PNP	3.9W
100M Half	0.19A	0.342W	0.02A	0.15A	0.49A	1.18W		3.882W
100M idle			0.02A	0.15A	0.49A	1.18W		3.54W
10M Full	0.19A	0.342W	0.02A	0.06A	0.92A	1.8W		5.742W
10M Half	0.18A	0.324W	0.02A	0.06A	0.92A	1.8W		5.724W
10M idle			0.02A	0.06A	0.42A	0.9W		2.7W

Note 1: Total power = power1 + 3 X power2. Note 2: Idle state is only based on IP108 power consumption.

For example: 24 ports 100 full mode power consumption = 0.360W+1.18Wx3 = 3.9W

1.2.2 Switching regulator selection

The specification of 34063 is recommended to be 4A@1.8v to meet the requirement. It is note that the efficiency of a switching regulator consisting of 34063 is about 65%

1.3 Power module selection

Refer to the power consumption listed in section 1.1 and 1.2, the recommended specification of power module is shown in the following table.

System	Power module		
	3.3V/ 2.5A	3.3V/ 4A	3.3V/ 5A
24 port dumb		OK	
24 port+1 web +1 fiber		OK	OK (recommended)
24 port dumb+2 fiber			OK
16 port dumb	OK		
16 port+1 web+1 fiber	OK	OK (recommended)	
16 port dumb+2 fiber		OK	

1.4 De-couple capacitor selection

For best system performance, MLCC capacitors are recommended.

	22uF MLCC	100uF E/C
IP1726 (1718) VDD33	OK	
IP1726 (1718) VDD18	OK	
IP108 VDDIO	OK	
IP108 VDDC	OK	
IP108 AVDD	OK	OK

Note1: IP108's AVDD is recommended to use 22uF MLCC+100uF E/C capacitors

1.5 Thermal Parameter

IP1726; IP1718: $\Theta_{ja}=38.2^{\circ}\text{C}/\text{W}$; $\Theta_{jc}=16^{\circ}\text{C}/\text{W}$

IP108: $\Theta_{ja}=29.1\sim 30.4^{\circ}\text{C}/\text{W}$; $\Theta_{jc}=10.7^{\circ}\text{C}/\text{W}$

2 SS-SMII and MII

2.1 SS-SMII driving current setting

For getting best system reliability, please refer to the suggested value in following table for I/O driving setting.

VDD33 of IP1716 = VDDIO of IP108 = 3.3V

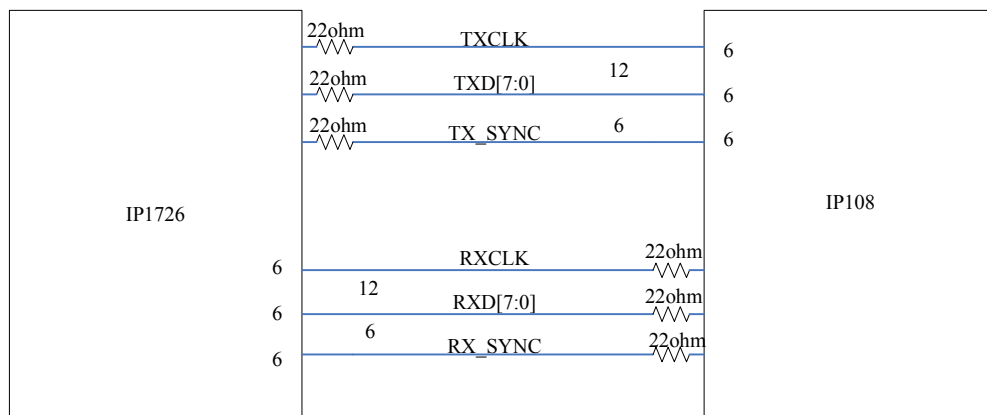
	1726(1718)_TXCLK	1726(1718)_TXSYNC&TXDATA	108_RXCLK	108_RXSYNC&RXDATA
Driving current	8mA	4mA	8mA	4mA
Setting	IP1726 (1718) pin 128, 123 setting = [0:0]		IP108 pin 60, 52 setting = [1:1]	

VDD33 of IP1716 = VDDIO of IP108 = 1.8V

	1726(1718)_TXCLK	1726(1718)_TXSYNC&TXDATA	108_RXCLK	108_RXSYNC&RXDATA
Driving current	12mA	8mA	12mA	8mA
Setting	IP1726 (1718) pin 128, 123 setting = [0:1]		IP108 pin 60, 52 setting = [0:1]	

2.2 SS-SMII termination

For impedance match and signal integrity, IP1726 (1718) and IP108 uses source termination scheme to reduce the signal reflection and EMI radiation. It is recommended to use TOP side of the PCB for SS_SMII signals and shouldn't use via to avoid degrading system performance. Termination resistors must be as close to the driver side as possible. The recommended value of damping resistors is 22 ohm. All recommended 22 ohm damping resistors are based on TXD (RXD) and TX_SYNC (RX_SYNC) 6 mils spacing, TX_CLK (RX_CLK) at least 12 mils spacing, SS_SMII signal trace width is 6 mils, no any via on SS_SMII signal trace ,and all SS_SMII traces on the top side of PCB.

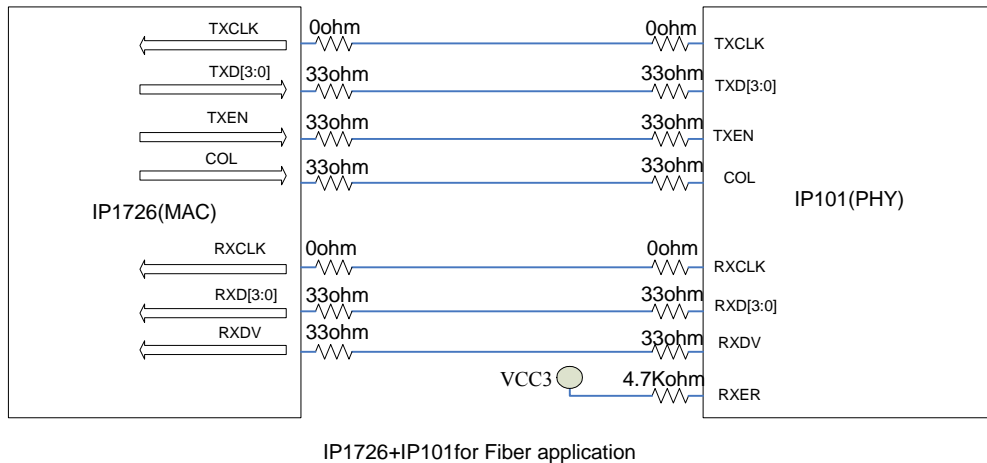
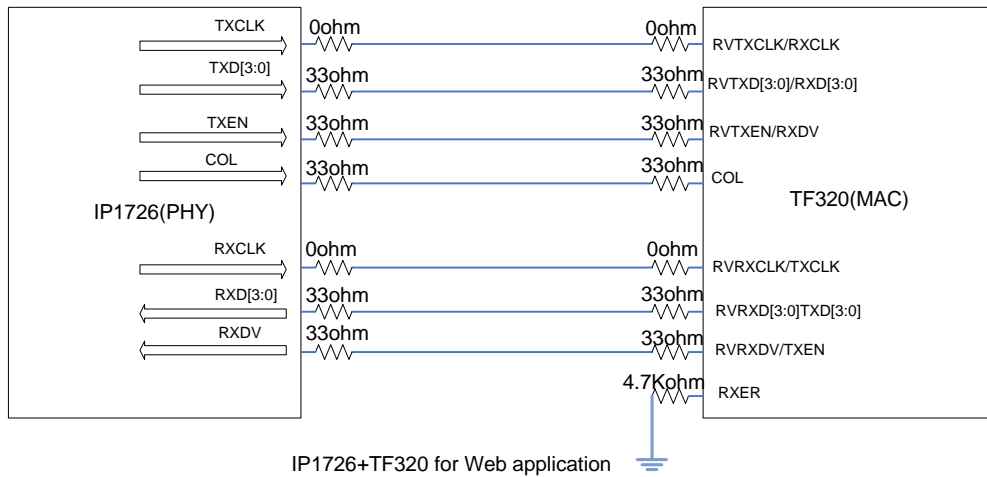


Unit: mil

2.3 MII termination

IP1726 (1718)'s two MII ports support Web or fiber applications. IP1726 (1718) is PHY mode and the Web controller is MAC mode in Web application. IP1726 (1718) is MAC mode and IP101 is PHY mode in fiber application. TF320 's RXER signal must be connected to ground through a 4.7Kohm resistor to prevent signal floating. IP101's RXER signal must be connected to 3.3v through a 4.7Kohm resistor to enable fiber mode.

IP1726 (1718)'s two MII ports use source/destination ends termination scheme, for example, in TX data and RX data paths, termination resistors are placed on source and destination sides. The recommended value of termination resistors is 33 ohm. IP1726 (1718)'s MII port TX_CLK and RX_CLK signals must be away from other signals for at least 12mil and only use discrete resistors for TX_CLK and RX_CLK.



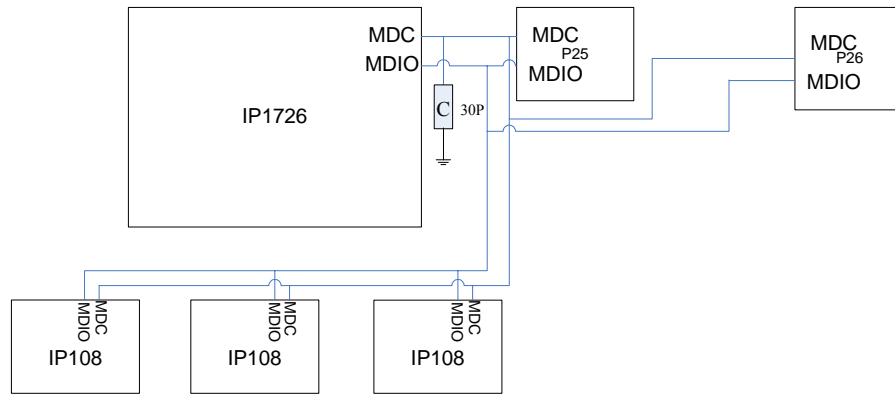
3 SMI and EEPROM

3.1 PHY address setting and MDC/ MDIO

IP1726 (1718) accesses PHY 's (IP108) registers by serial management interface, MDC and MDIO. The 24 ports PHY address should be set as 8-15(P0-P7), 16-23(P8-P15), and 24-31(P16-P23) in sequence, the 16 ports PHY address should be set as 8-15(P0-P7), 16-23(P8-P15), and the two MII ports are 5(P24) and 6(P25).

MDC/MDIO signals are shared by many chips. For better signal quality, a daisy chain topology is preferred.

MDC/MDIO signals should be away from other signals to prevent from interference. It is recommended to place a 30pF capacitor close to the MDC pin of IP1726 (1718) to reduce signal overshoot/ undershoot.



Daisy chain topology for MDC/MDIO layout

3.2 EEPROM

IP1726 (1718) uses a 24C08 to store configuration of Web. EEPROM is not necessary in a dumb application. IP1726 (1718) begins to reads EEPROM at the end of reset and it takes about 50ms. After finishing the read operation IP1726 is isolated from the EEPROM automatically. If the EEPROM is shared with an MPU, MPU should keep the EEPROM I/F to be Hi-z during the period which IP1726 (1718) accesses the EEPROM. Otherwise, it will cause IP1726 (1728) read error data and result in unpredicted result.

4 Reset circuit

In order to enhance system stable upon power on, it is recommended that use 100Kohm resistor and 0.1uF capacitor on RC reset circuit.

5 Layout consideration

For layout consideration, please refer to IP1726 (1718)+IP108 layout guide.